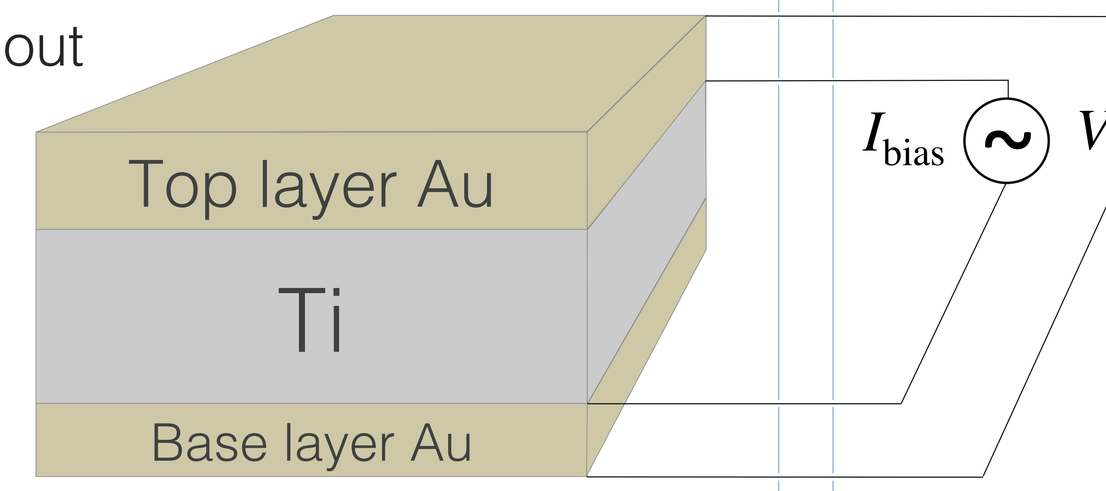
Tuning SPT-3G TES electrical properties with a trilayer Au-Ti-Au thin-film stack

Faustin W. Carter on behalf of the SPT-3G Collaboration

Argonne NATIONAL LABORATORY

Trilayer film geometry

- Au-Ti-Au trilayers sputtered without breaking vacuum
- SiN substrate
- 5 nm Ti glue layer under base

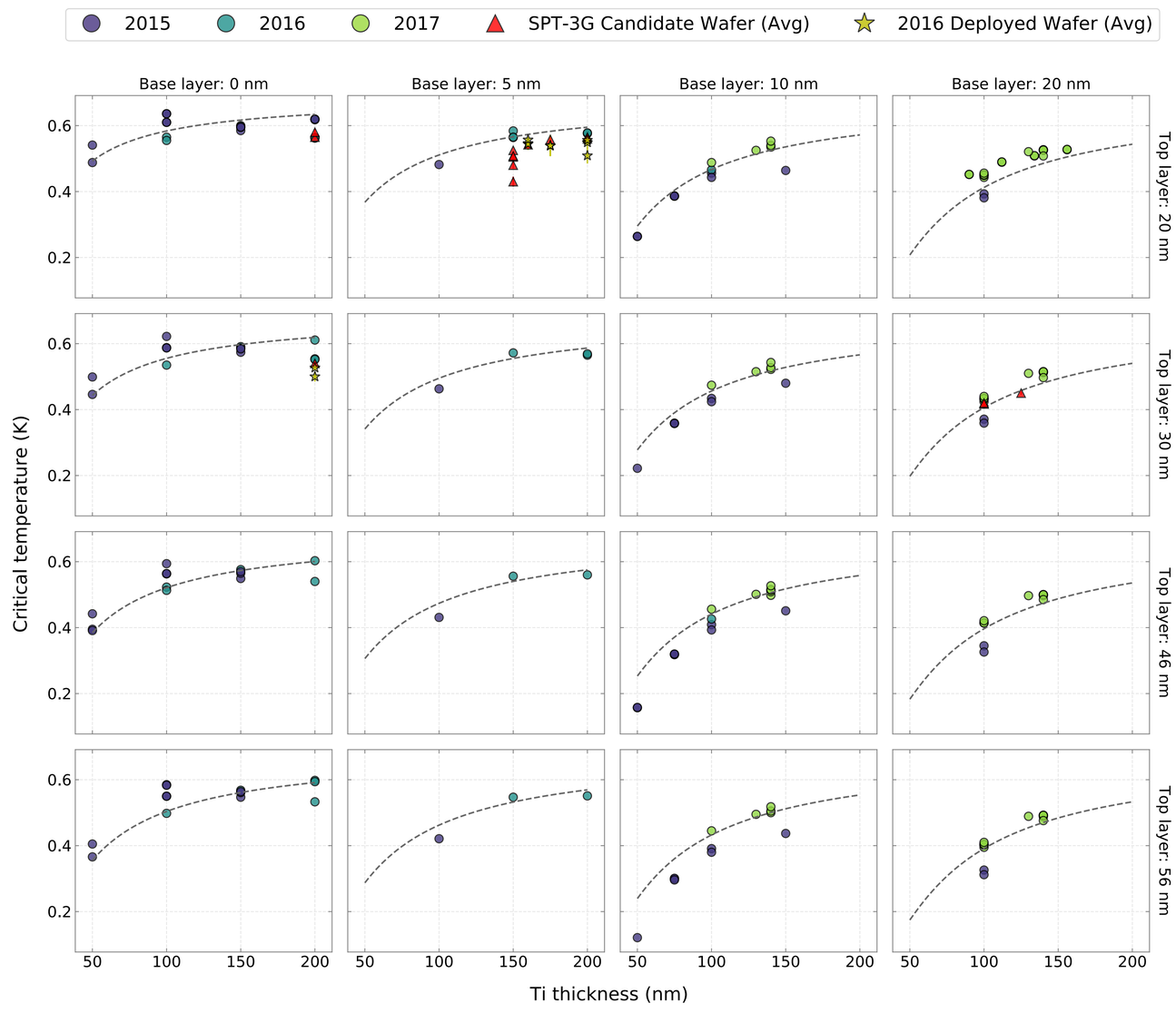


Measurement

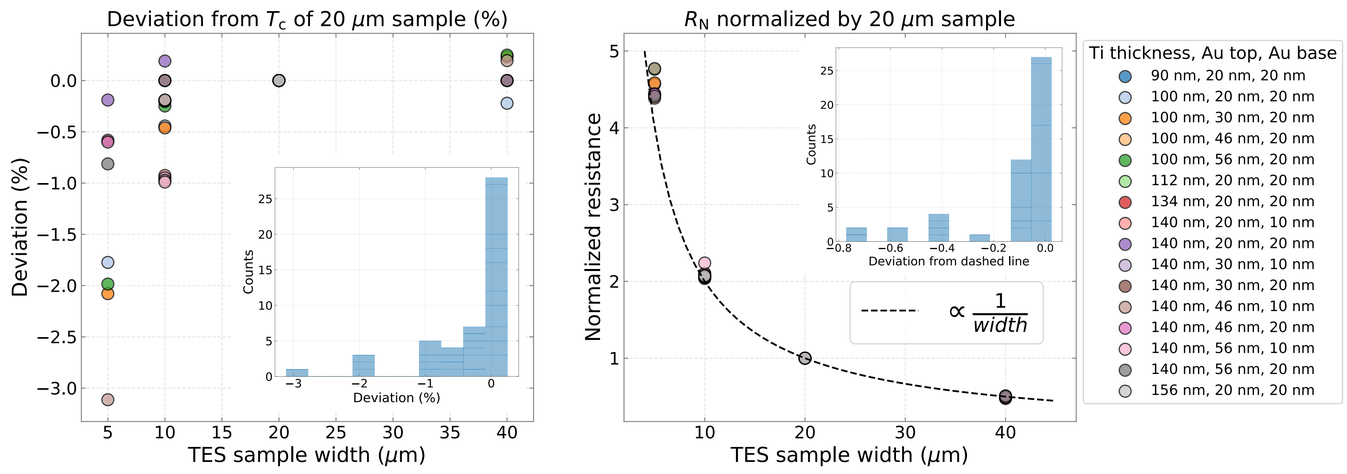
- ADR cryostat used to sweep temperature (0.1–0.7 mK)
- Four-wire resistance measured with AC bridge
- Temperature measured with RuOx sensor

Trilayer T_c dependence on film thickness

- Au-Ti-Au trilayer is modeled as a Au-Ti bilayer with an effective Au thickness that is a linear combination of trilayer Au thicknesses: $d_{\mathrm{eff}} = d_{\mathrm{Base}} + w\, d_{\mathrm{Top}}$
- Usadel equations used to fit all data with only three free parameters:
  1. Ti T_c with no Au (680 mK)
  2. Effective $R_{\mathrm{interface}}$
  3. Top layer weight factor w
- Effective bilayer Au thickness (d_{eff}) result is: $d_{\mathrm{eff}} = d_{\mathrm{Base}} + 0.16\, d_{\mathrm{Top}}$
- Systematic T_c offsets with different sputtering targets (labeled by year)



Trilayer T_c, R_N dependence on sample width



- T_c weakly depends on TES width
- R_N scales inversely with TES width

Resistance may be tuned entirely by width without regard to film thickness.

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