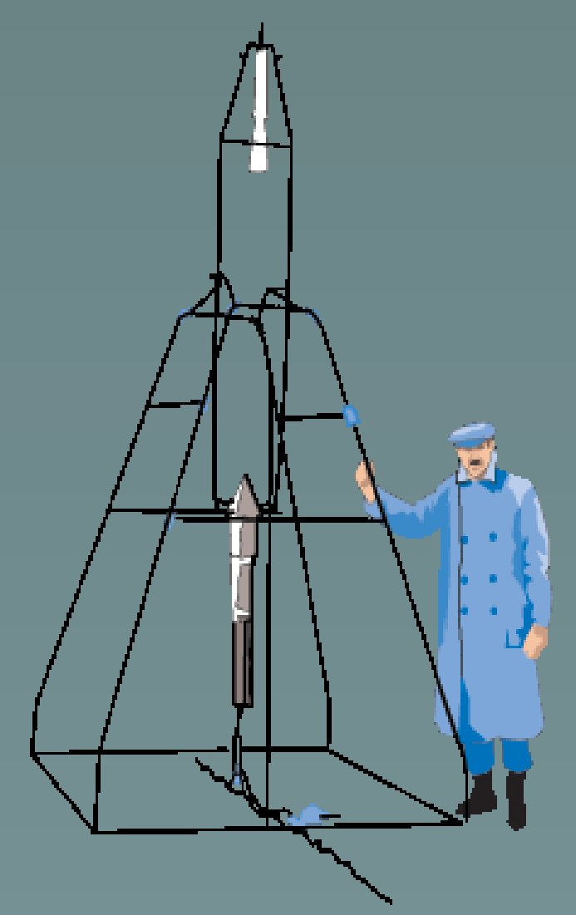
# Fabrication of Flexible Superconducting Wiring with High Current Carrying Capacity Indium Interconnects



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## ABSTRACT

The X-ray Integral Field Unit (X-IFU) is a cryogenic spectrometer for the Advanced Telescope for High Energy Astrophysics (ATHENA). ATHENA is a planned next-generation space-based X-ray observatory with capabilities that surpass the spectral resolution of prior missions. Proposed device designs contain up to 3840 transition edge sensors (TES), each acting as an individual pixel on the detector, presenting a unique challenge for wiring superconducting leads in the focal plane assembly. In prototypes that require direct wiring, the edges of the focal plane on the instrument have hosted aluminum wire bonding pads; however, indium 'bumps' deposited on an interface layer such as molybdenum nitride (MoN) can instead be used as an array of superconducting interconnects. We investigated bumped MoN:In structures with different process cleans and layer thicknesses. Measurements of the resistive transitions showed variation of transition temperature $T_C$ as a function of bias and generally differed from the expected bulk $T_C$ of In (3.4 K). Observed resistance of the In bump structures at temperatures below the MoN transition (at 8.0 K) also depended on the varied parameters. For our proposed X-IFU geometry (10 microns of In mated to a 1 micron In pad), we measured a $T_C$ of 3.1 K at a bias current of 3 mA and a normal resistance of 0.55 mΩ per interconnect. The design and fabrication of superconducting niobium (Nb) microstrip atop flexible polyimide was also investigated. We present a process for combining In bumps with Nb on polyimide to enable high density wiring for the X-IFU focal plane.

## Need for high $I_C$ flexible interconnects on x-ray focal planes

Prototype for dc bias option for detector scalable to size of ATHENA X-IFU focal plane

X-IFU consists of up to 3840 TES microcalorimeter sensors requiring mA bias levels (for complete calibration)

Wirebond pad area is prohibitive

Indium replacement for wirebonds feasible :

No Heat - absorber cannot withstand post bump anneal.

On-chip structures shorter than absorbers for fabrication process compatibility (we have chosen 1 micron for the mating Indium

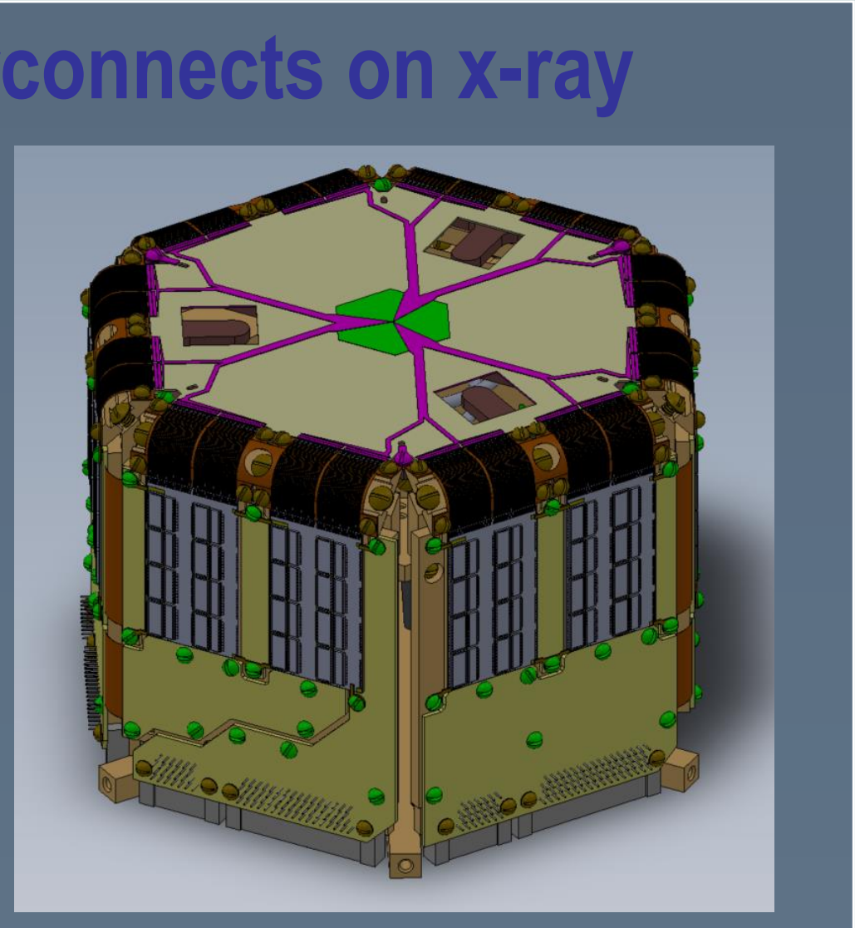


*Fig. 1 X-ray focal plane prototype connected to bias circuit/readout via "around the corner" flexible circuit boards (Figure courtesy Randy Doriese)*

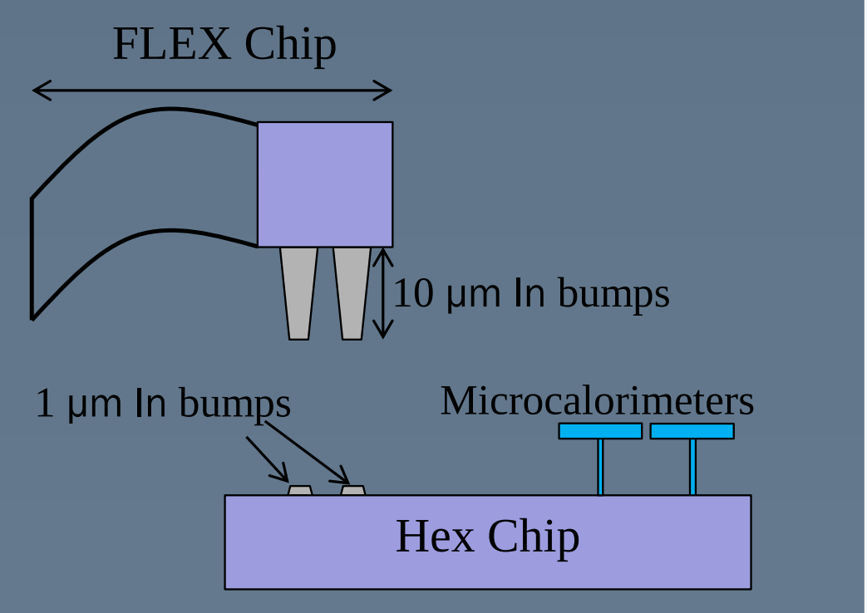
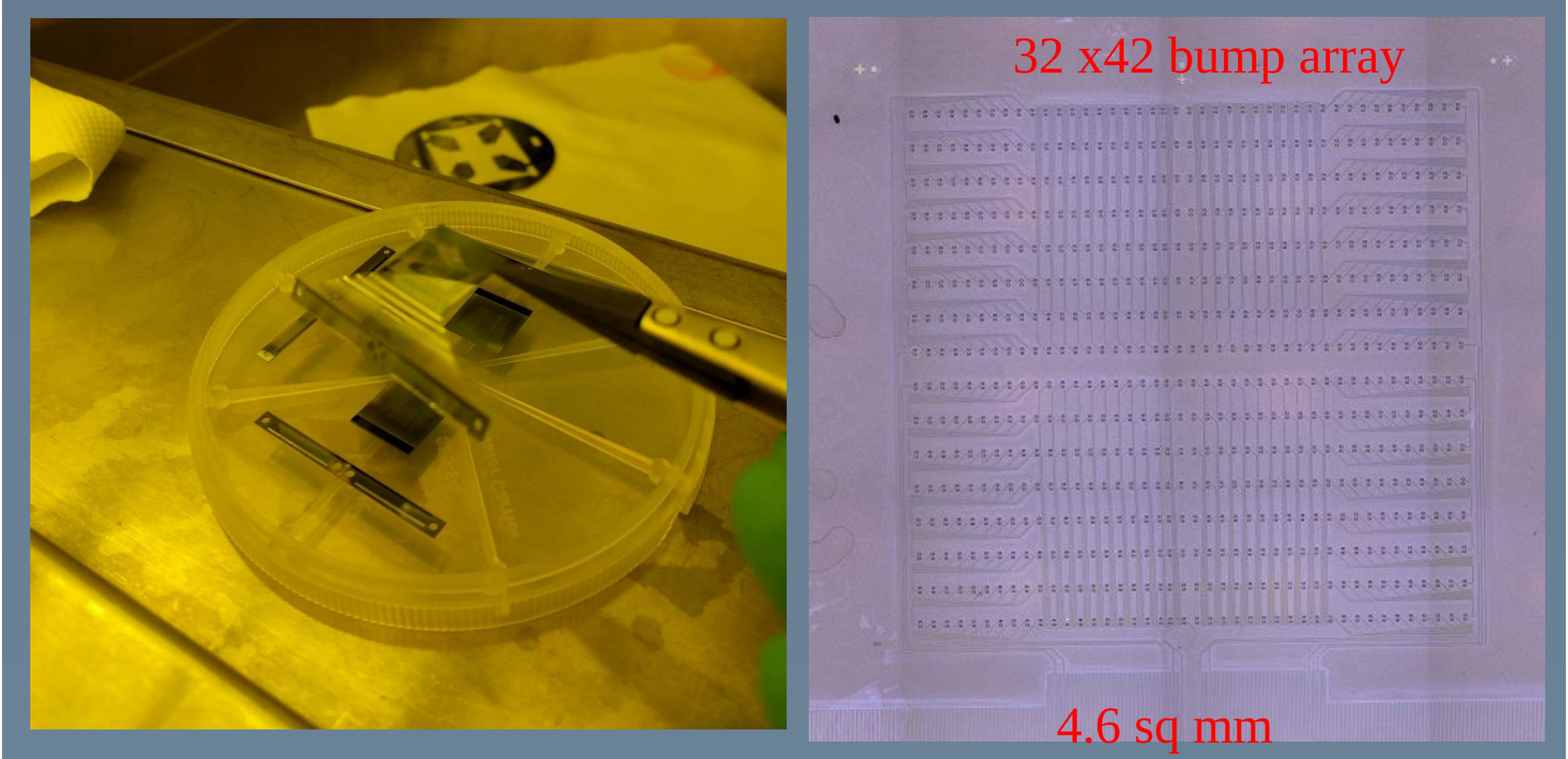


*Fig. 2: Depiction of mating of detector chip to flex cable with Indium bumps. 2 sided process with 10 micron bump to 1 micron bump is explored here*

## FABRICATION OF INDIUM PLUS FLEX



Polyimide flex successfully integrated with superconducting Nb microstrip and 10 micron indium liftoff. Left side shows completed chip. Right side is a detail of the array of indium bumps fully wired out across "flex" region (1260 bumps to 630 wire pairs)

### FABRICATION OVERVIEW: FLEX CHIP

Polyimide spun onto oxidized silicon and cured (~6 micron thick)

Poly is etched with CF4/O2 to slope sidewall ~45 degrees

Deposit and Pattern wiring (Ti/Nb/Ti) including MoN capping layer

Top layer of polyimide(~6 microns) is cured and patterned

10 microns indium deposited through image reversed liftoff mask

Wax mounting of indium (120 C wax press) followed by deep etch

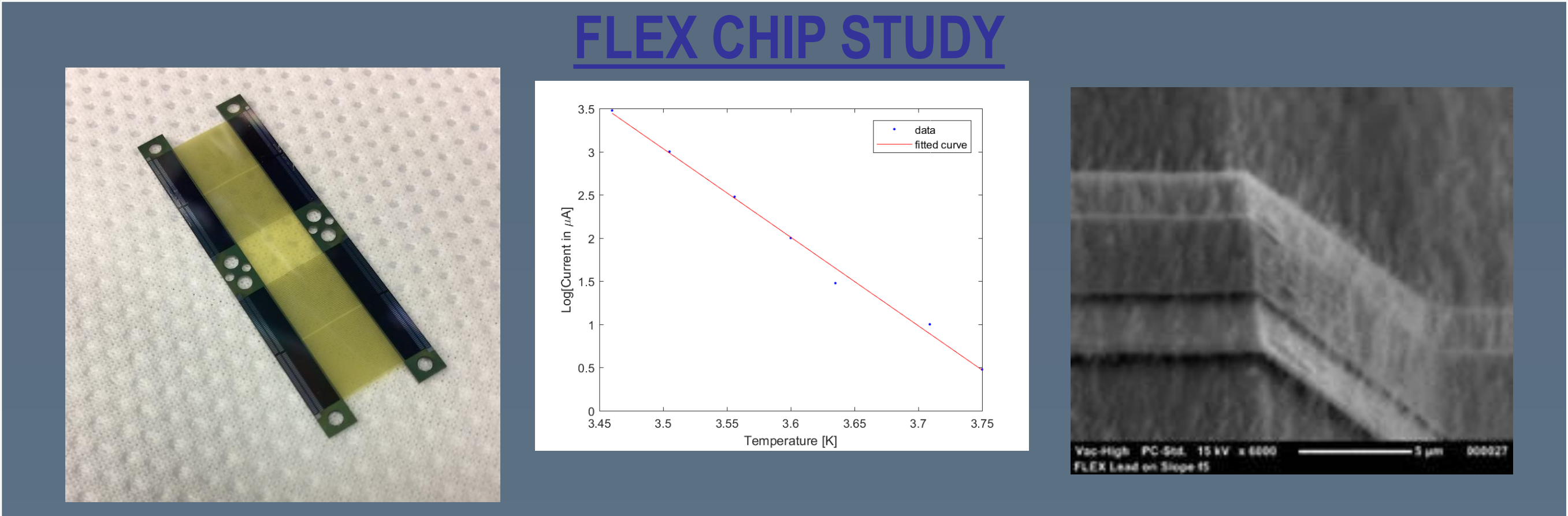
### HEX CHIP FABRICATION

Detector fab is routine and Indium adds two steps for MoN dep and Pattern followed by Indium liftoff (to 1 micron thickness)

Absorber deposition follows the indium liftoff – restricting In height So 3 micron photoresist will cover them during electroplating

If Bi is used in absorber, heat restriction (120 for short time) and gentle clean prior to bumping (such as ONTOS downstream plasma) is indicated / preferred.

## FLEX CHIP STUDY



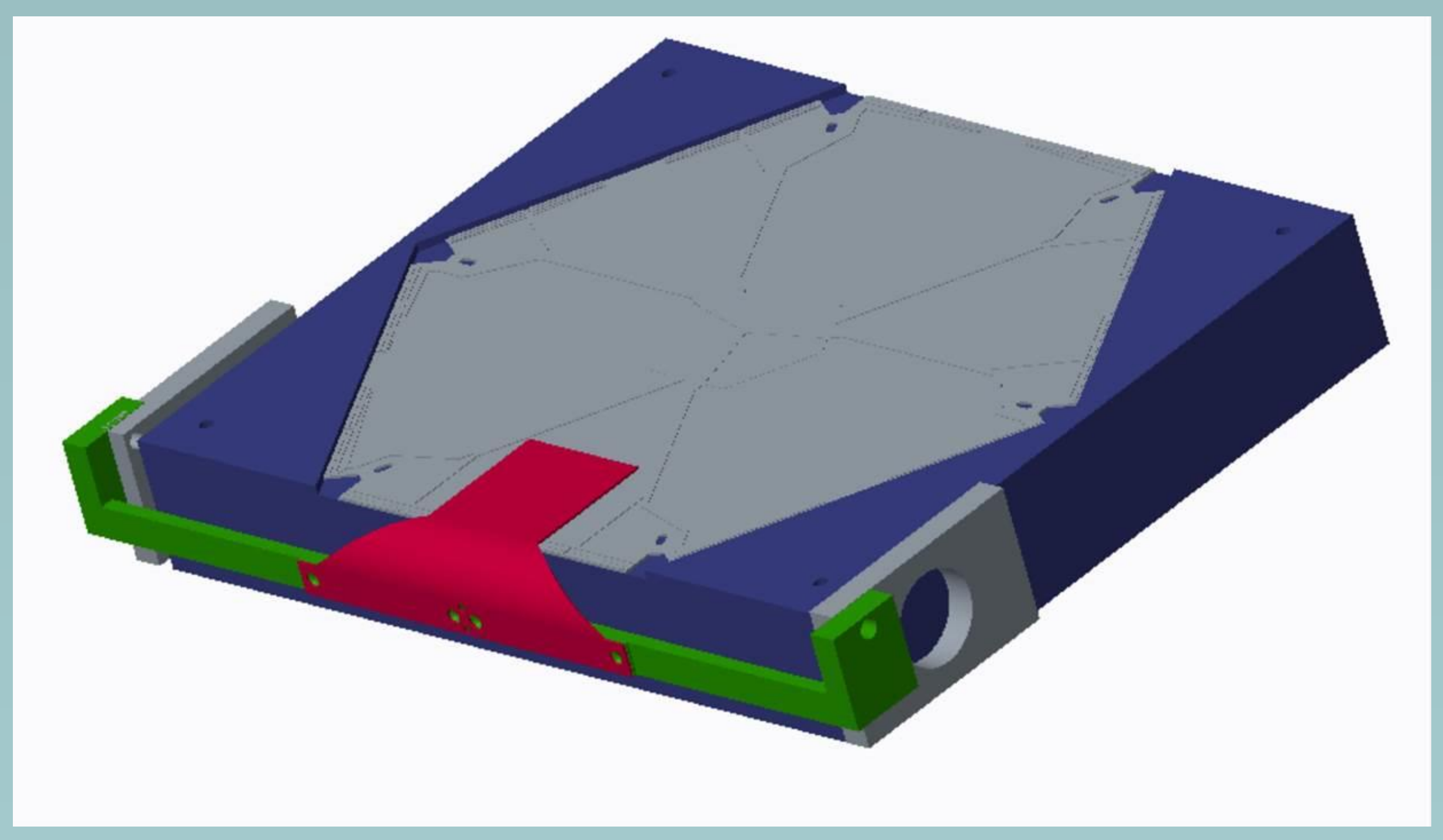
*Left – Superconducting microstrip flex with wirebond padssuitable for integration into X-IFU prototype FPA; Center – Critical current >5 mA demonstrated; Right – SEM of sloped region currently limiting measured critical current*

Ti/Nb/Ti doublestrip wiring sandwiched between 6 micron layers of polyimide.

$CF_4$ plasma to etch lower poly layer with sloped sidewall. Indium bumps or wirebond pad on Si (no poly) regions

Low $I_C$ (estimated to be 6 mA) currently dominated by transition at sidewall. Other Nb regions show 9 K Tc when folded 90 degrees

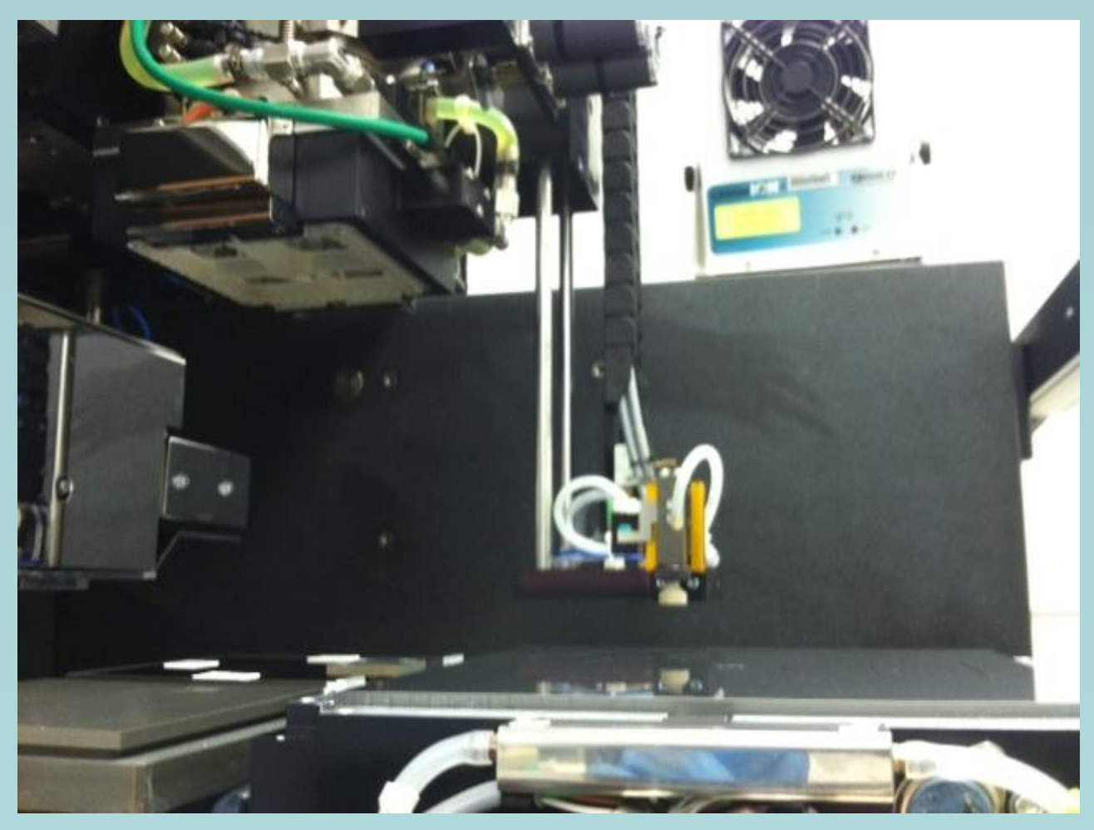
## ASSEMBLY CONCEPT

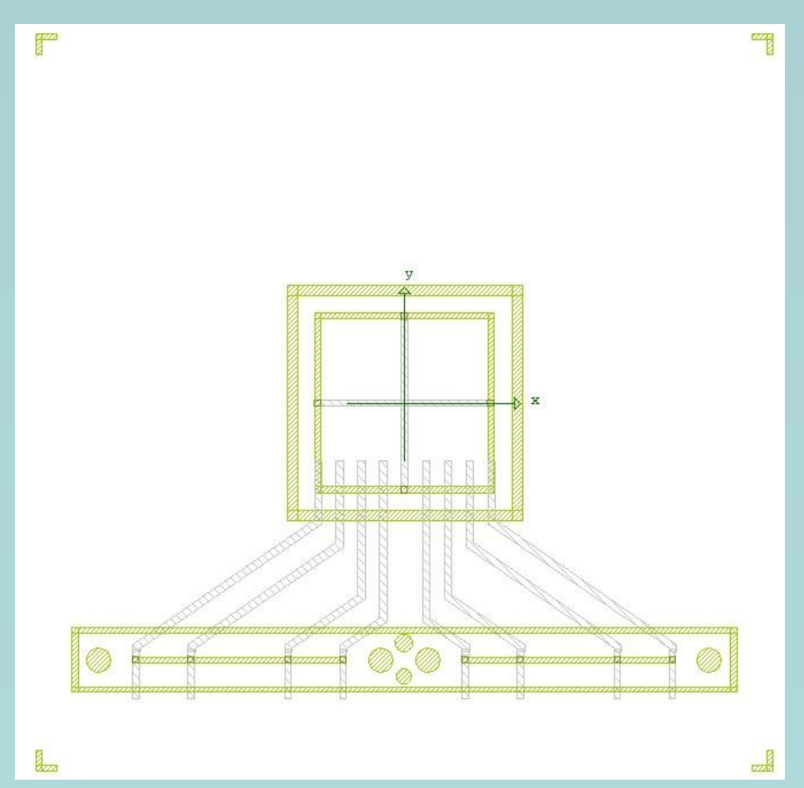


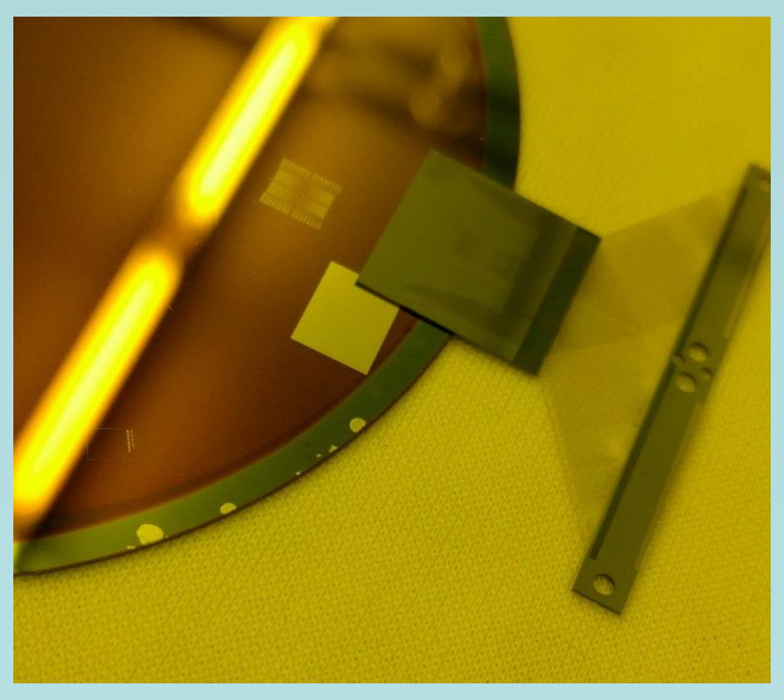
CAD design for bump-bonded hex-to-flex testbed. Prototype silicon parts are in fabrication

Hex chip will have 90 mm diameter – 6 regions with indium bump fields with ~1260 bumps per region (plus support bumps to increase joint strength)

Flex chip is 1.5 cm sq with fanout to 4.5 cm chip for initial wirebond tests of circuit. Second side of chip will eventually be bumped to readout card in full assembly.





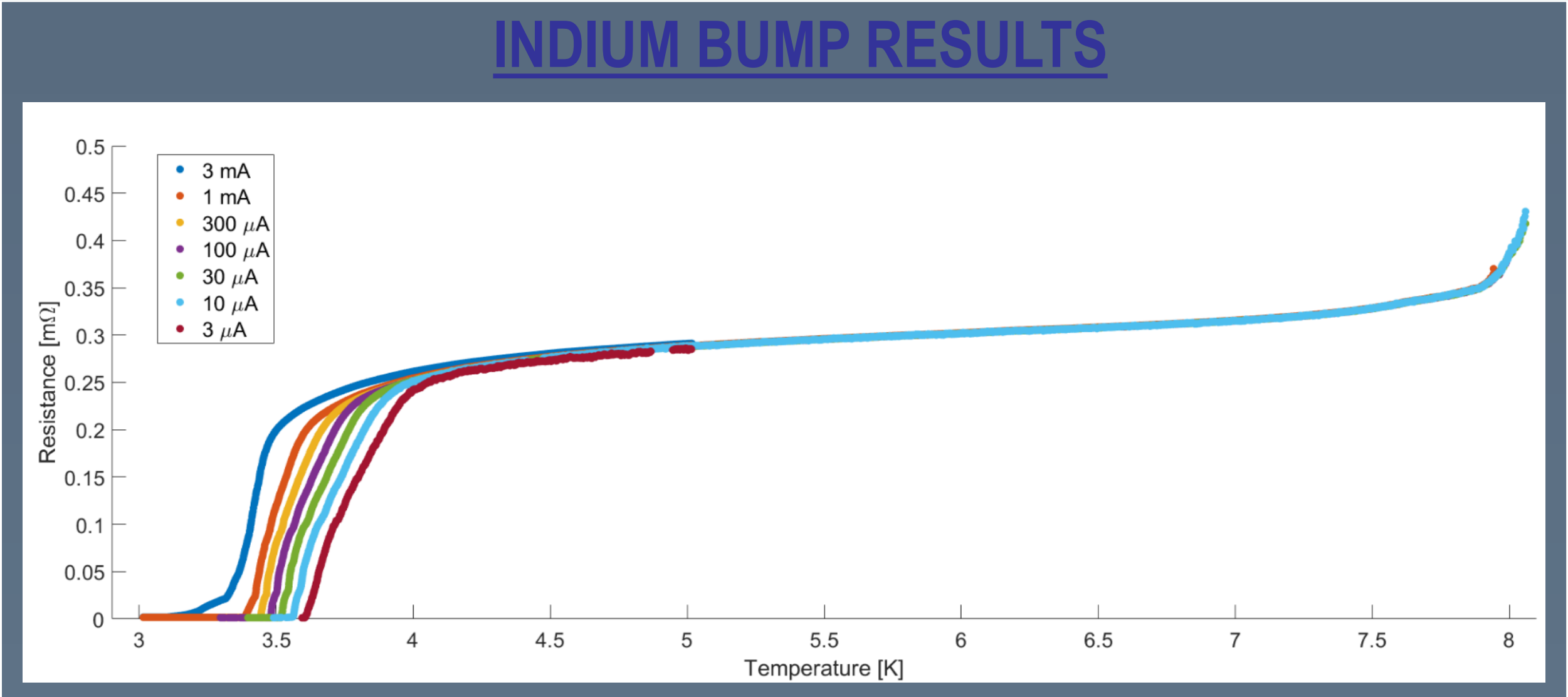


Flip chip bumpbonder (4 inch top plate / 6 inch base plate)

Vac interface plate uses to lift flex chip

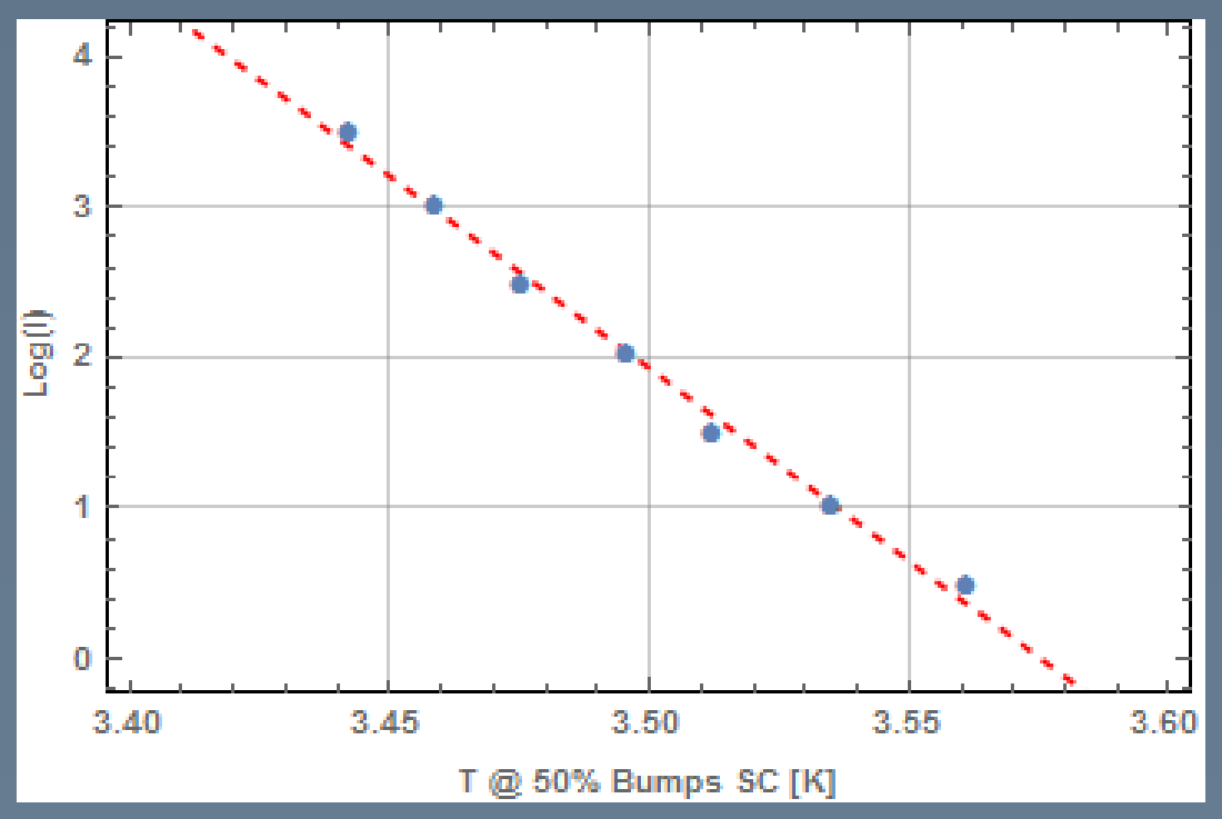
Indium bump region is sub-cm for X-IFU scale

## INDIUM BUMP RESULTS

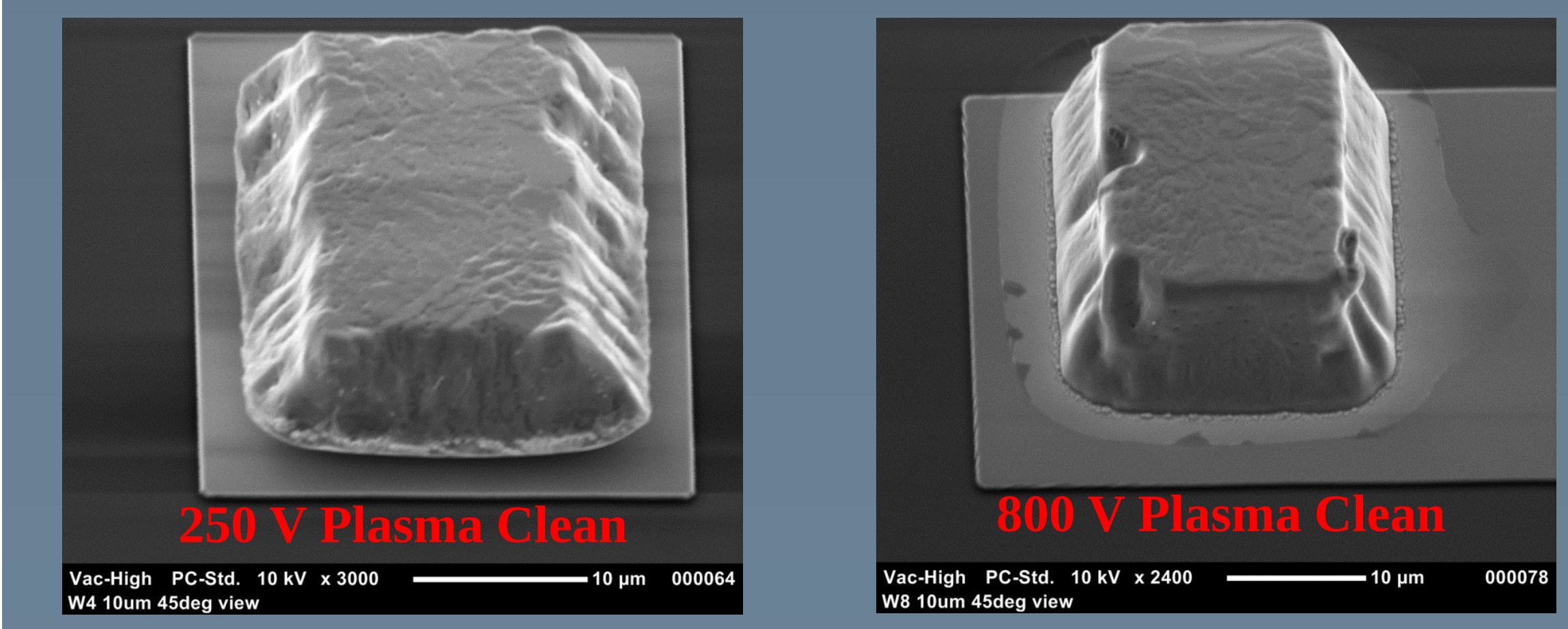


Resistance versus temperature of bumped 10:1 micron indium coupons at different excitation. The R(T) at the highest excitation (3 mA) exhibited $T_C$ above 3 K.

### CURRENT CARRYING CAPACITY



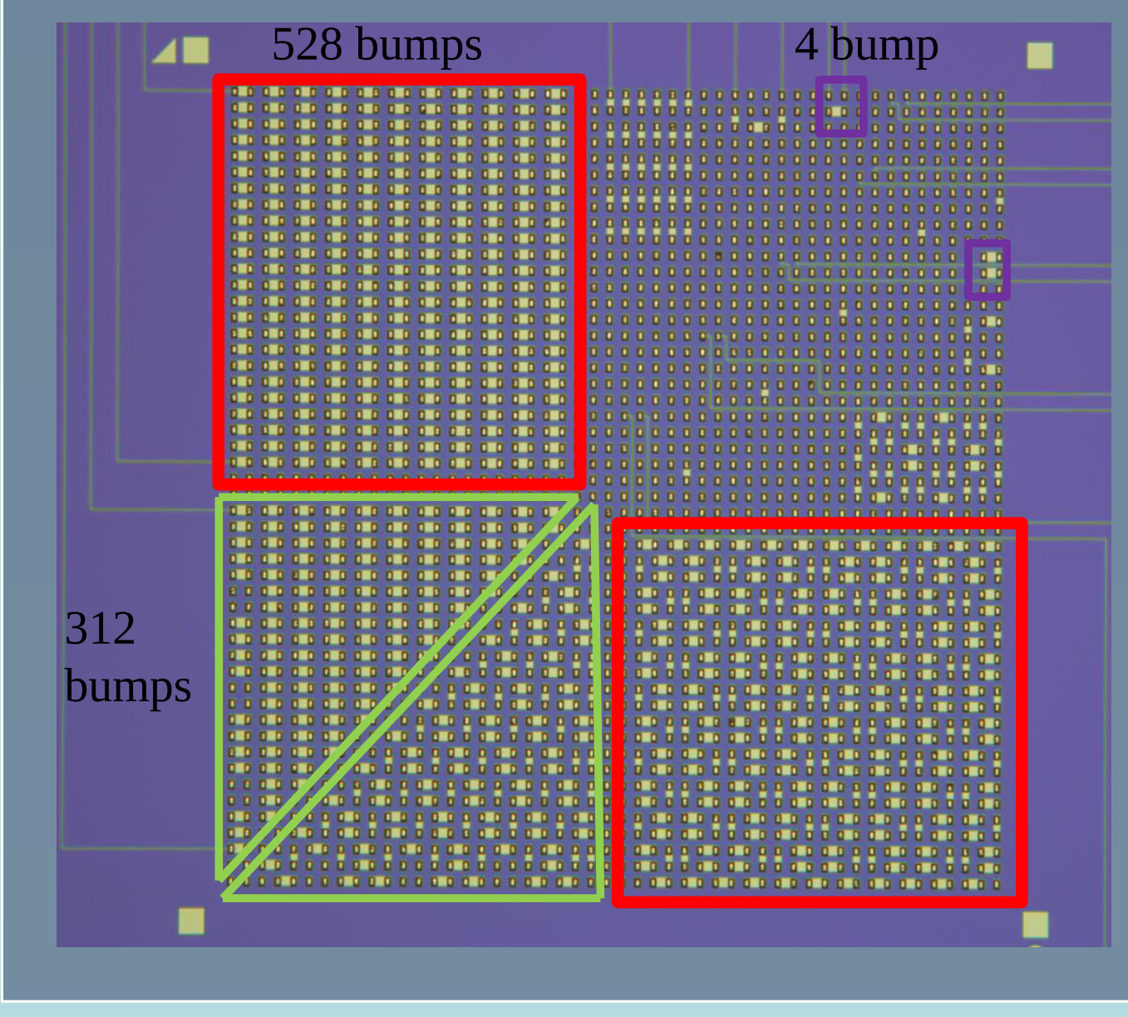
Tc drops linearly with bias current in R(T) curves and indicates a high low-temperature critical current for MoN:In 10:1 indium bumps cold pressed with no post bump anneal process applied



*Left –10 micron In bump from MoN following 250 V substrate preclean. Right – 10 micron In bump following 800 V clean. Despite the different appearance, yields were similar, though bump resistance varied by a factor of ~3 in different 10:10 bump coupons*

| Bump Thicknesses [µm] | Sample Cleans for Bump Interfaces (MoN:IN / In;IN) | $T_C$ @ 3 mA | $R_{bump}$ @ < 8K |
|---|---|---|---|
| 1:10 | 800 V / ONTOS | 3.46 K | 0.54 mΩ |
| 10:10 | 250 V / RIE | 3.44 K | 0.13 mW |
| | 800 V / ONTOS | 3.44 K | 0.04 mΩ |

Summary of bump $T_C$ and $R_n$ for different bump geometries and sample cleans use of 1 micron bump increases $R_n$ 5-15x over thicker film bumps but $T_C$ ($I_{bias}$) is similar for both geometries



Symmetric chip for In test coupons

3 bumped assemblies received different precleans, film thicknesses and postcleans (prior to bumping)

"ONTOS" clean is a downstream plasma surface process that will be more gentle to the absorbers than the RIE process that uses sputtering to remove InOx from the bumps

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