SUPERCONDUCTING MULTILAYER HIGH DENSITY FLEXIBLE PCB FOR VERY HIGH THERMAL RESISTANCE INTERCONNECTIONS

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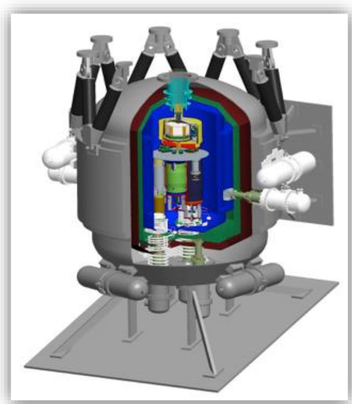
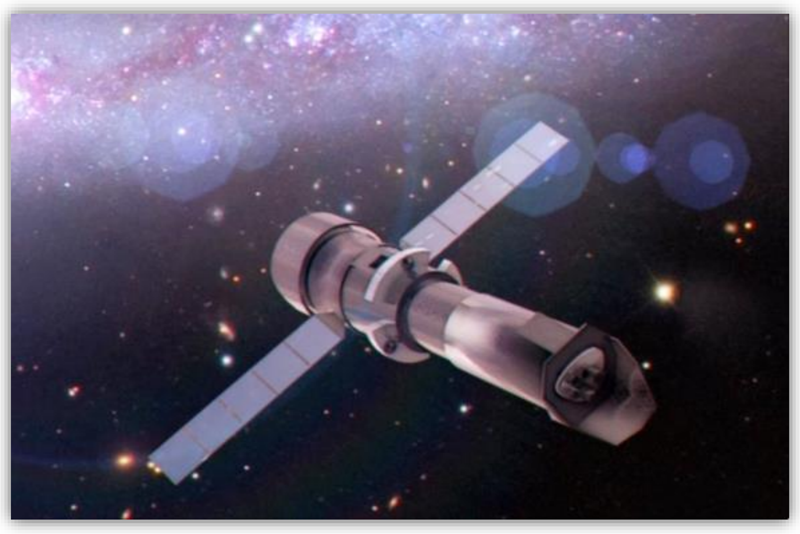
Context

- **Very low temperature detectors** (50 mK to 1 K).
- **Space instruments** : X-IFU of Athena satellite, R&D MicroCal-X, SAFARI of SPICA satellite (?) or **terrestrial instruments** : Artemis of APEX telescope in Chili.
- **High impedance** sensors (Si-doped thermometers or high resistivity TES) or **low impedance** sensors (TES thermometers).
- **Funding** :
  - European space agency (ESA),
  - French space agency (CNES),
  - European commission





Athena+ (right), the future international X-ray spatial observatory, and X-IFU (top), a X spectro-imager made of micro-calorimeters

Needs

- **To interconnect very cold detectors** (typically 50 to 300 mK) **to less cold stages** (typically 2.5 to 4 K), that contain either cryo-electronics, or simply intermediary cold source.
- **To readout highly segmented detectors** (typically 4000 pixels cameras) which requires thousands of tracks.
- **To minimize thermal charge** on coldest stage.
- Possibly to **shield** signal lines.

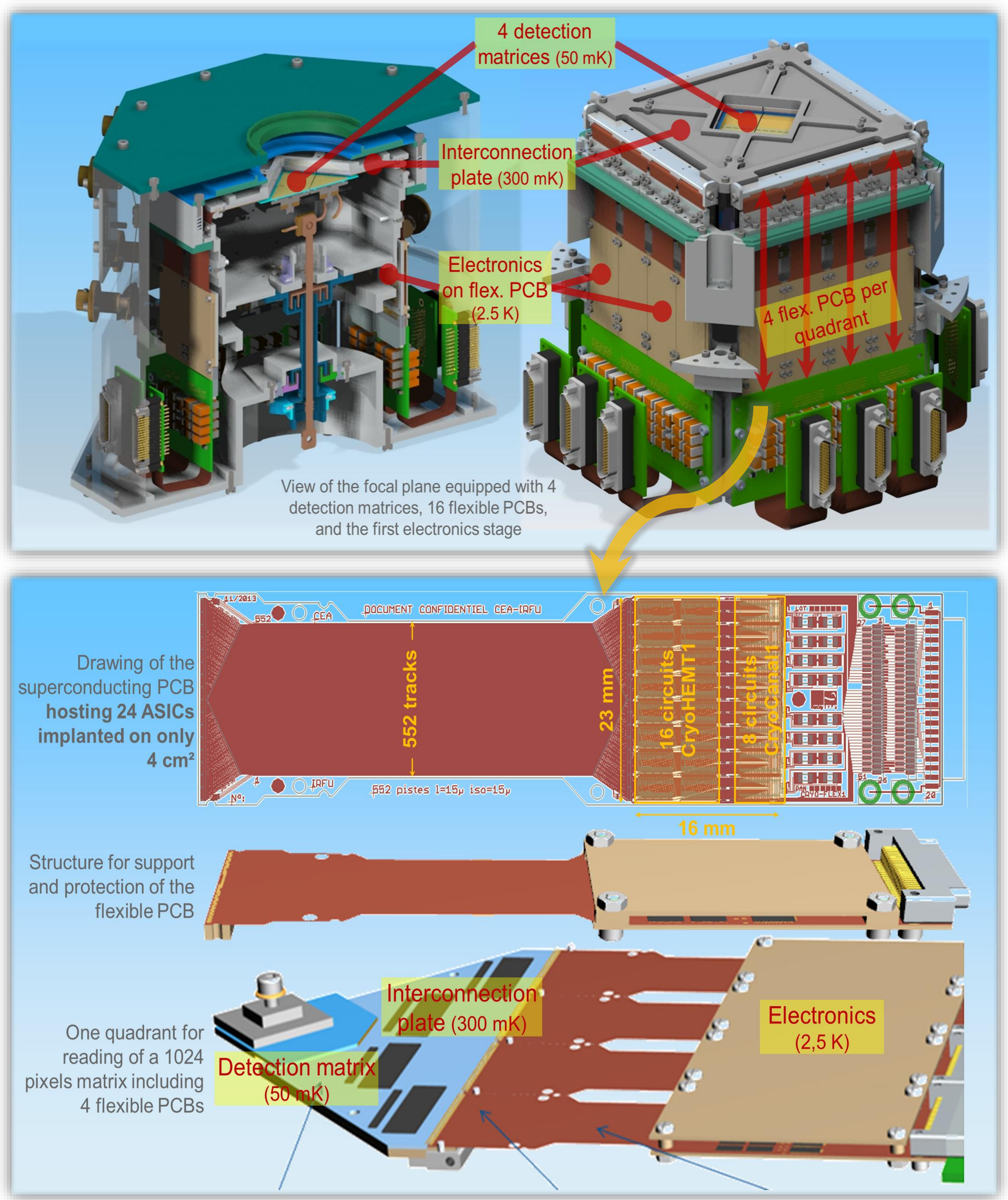
Our solution

- **Very thin polyimide** support : 17 to 34 µm.
- **Very narrow tracks** – until 10 µm – to minimize flex width.
- **Superconducting metal** – niobium – to maximize tracks thermal resistance.

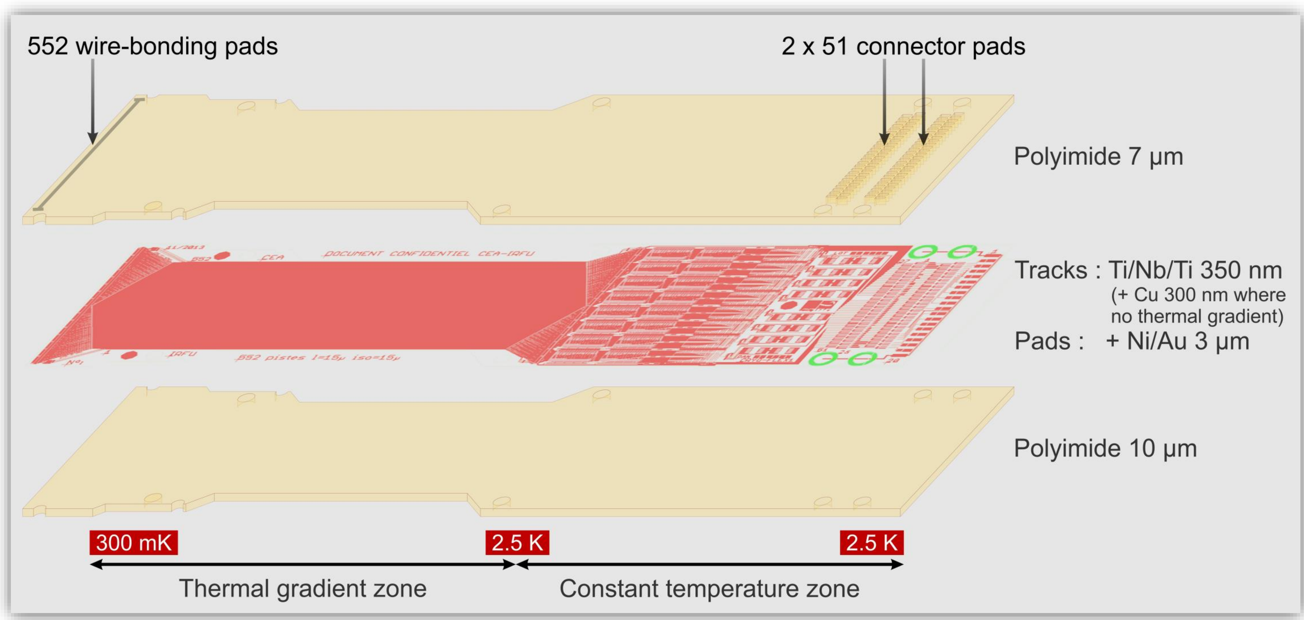
⇒ Minimize the flex thermal conductance

- **Chips on flex** (first realization) in case of (multiplexing) cryo-electronics, to benefit from the very large integration level permitted by the narrow tracks.
- **Multilayer flex** (second realization) if shielding is needed.
- **Collaboration** : – design and tests : **CEA/IRFU** – manufacturing : **Hightec MC AG**

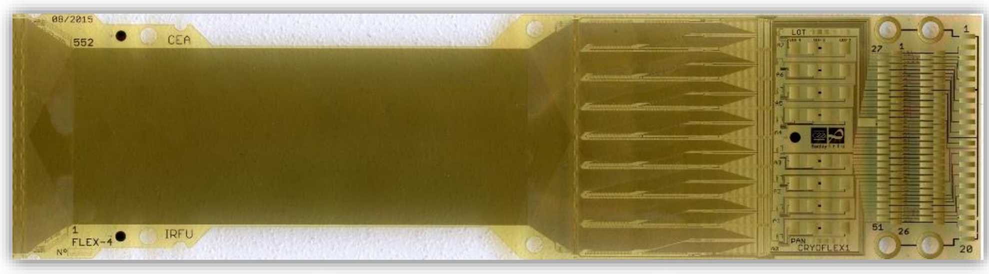
First realization : monolayer flexible PCB with chips on flex

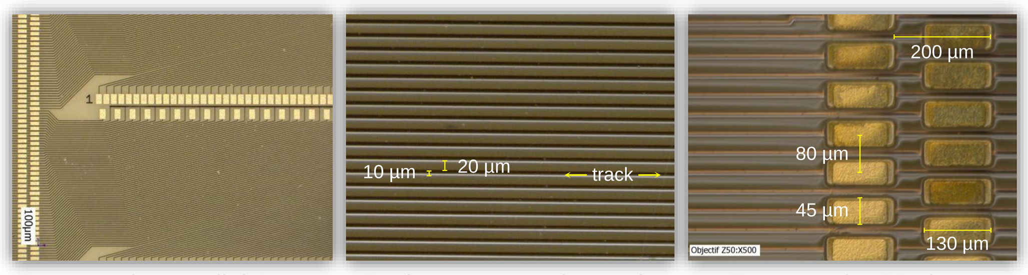


- **Functions of flexible PCB :**
  - To interconnect the detector (50 mK) to the cryo-electronics (2.5 K) via an interconnection plate (300 mK).
  - To implement the 24 integrated circuits of the pre-amplifying and multiplexing cryo-electronics.
- **Features :**
  - A thermal gradient zone (300 mK to 2.5 K) with superconducting tracks, and a constant temperature zone (2.5 K) with coppered superconducting tracks.
  - In thermal gradient zone : 552 tracks : width : 10 µm, space : 20 µm.
  - In constant temperature zone : 24 wire-bonded chips on a 23 mm x 16 mm area.
  - Interconnections :
    at input side, 552 wire-bonding pads (pitch 80 µm in 2 staggered columns = pitch 40 µm) ;
    at output side, a 51 points SMD Nano-D connector (23 mm width).
  - Flexible PCB dimensions : l x w = 90 x 23 mm.
    Thermal gradient zone : l x w = 25,83 x 17 mm. Depth = 17 µm.



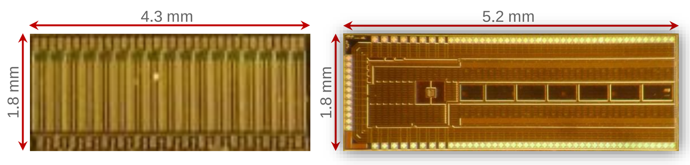
- **Pictures of the realizations :**





Zoom on the parallel 10 µm-tracks and on the pads. *Further zoom on the tracks (10 µm width, 20 µm space).* *Zoom on the 552 input wire-bonding pads.*

The circuits to implement : 16 x Cryo17HEMT1 (by CNRS/LPN) and 8 x CryoCom1 (by CEA/IRFU)



2 circuits ready to be bonded. *2 CryoCom1 circuits wire-bonded on the flexible PCB.*

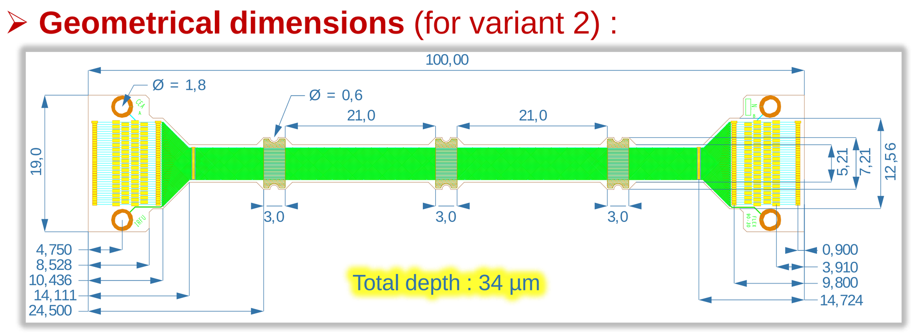
- **Next steps :**
  - Bonding of all circuits, and soldering of the SMD Nano-D connector.
  - Integration in the acquisition chain.

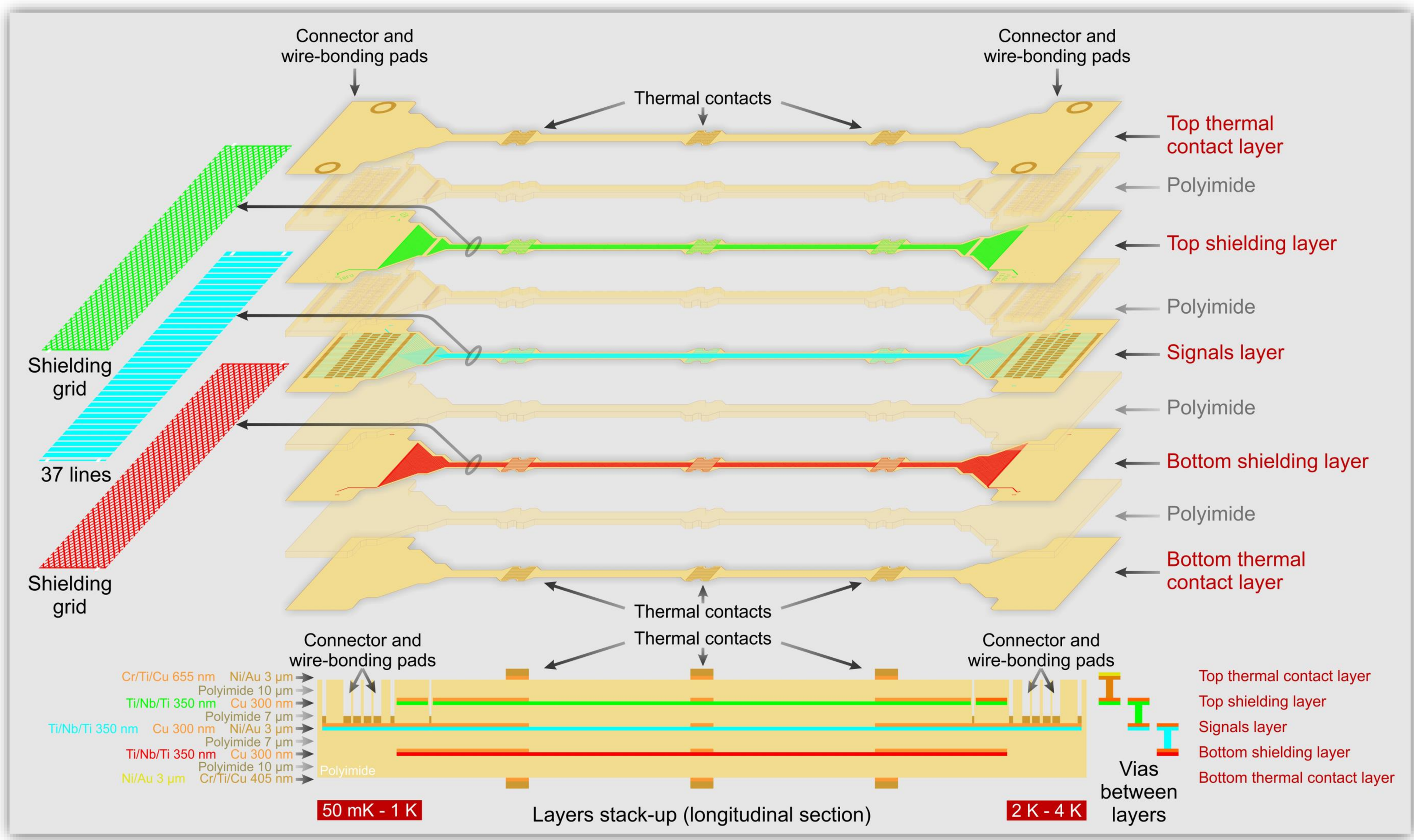
Second realization : multilayer flexible PCB for shielded interconnections

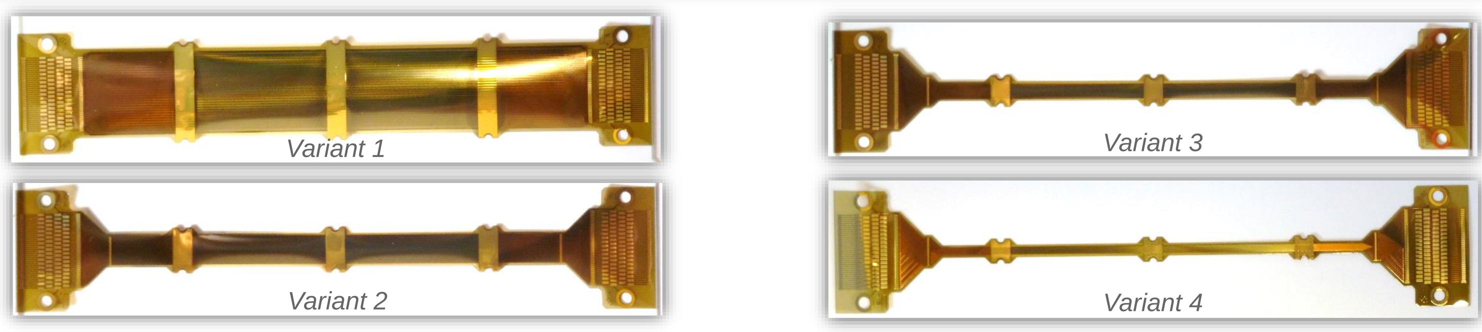
- **Function :**
  Generic superconducting harness for readout of very low impedance detectors (like TES) or high impedance detectors (like Si-doped thermometers or high-resistivity TES).
- **Features :**
  - 37 tracks, 3 electrical layers + 2 thermal layers.
  - Signals layer intercalated between 2 hatched shielding plans, all grounds being connected by vias.
  - Interconnection : either by SMD NanoD connectors, or by wire-bonding (if very low contact resistance or maximal compactness is needed).
  - Four variants, with different tracks width and space : 15 µm (spaced by 15 µm), 30 µm (spaced by 30 µm), 90 µm (spaced by 30 µm), 300 µm (spaced by 100 µm).
- **Theoretical performances of each variant :**

Characteristics and theoretical performances	Variant 1	Variant 2	Variant 3	Variant 4
Tracks width (µm)	300	90	30	15
Tracks spacing (µm)	100	30	30	15
Shielding filling ratio	0,25	0,5	0,5	0,5
Tracks quantity	32	37	37	37
Minimal harness width (mm)	14,1	5,21	2,99	1,89
Total thermal conduction (W/K)	**1,45E-07**	**6,08E-08**	**2,95E-08**	**1,77E-08**
Critical current at 4 K (mA)	**105**	**31,5**	**10,5**	**5,25**

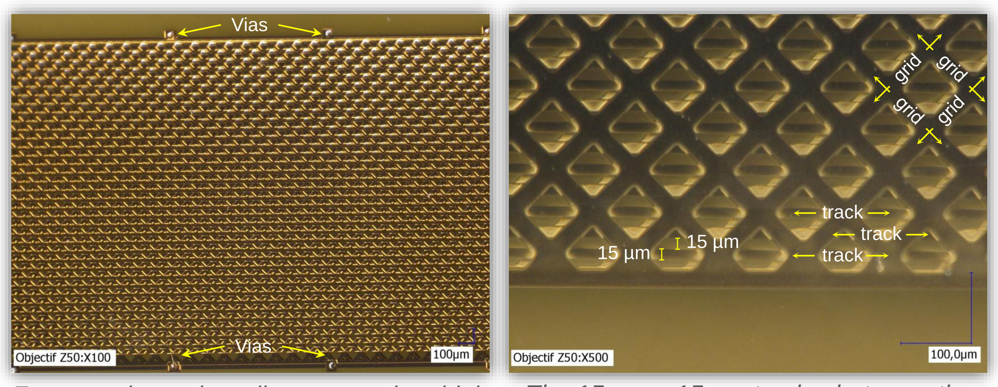
- **Geometrical dimensions** (for variant 2) :



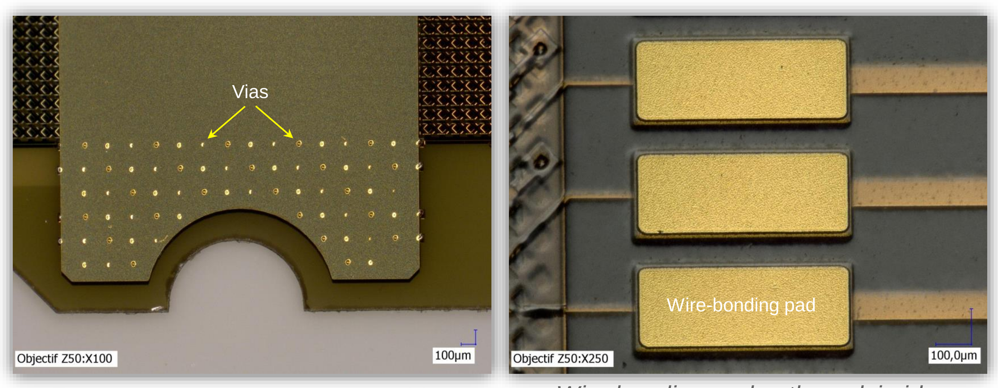




- **Pictures of the realizations :**



Zoom on thermal gradient zone ; the shielding grids are closed by vias (Variant 3). *The 15 µm – 15 µm tracks, between the two shielding grids (Variant 4).*



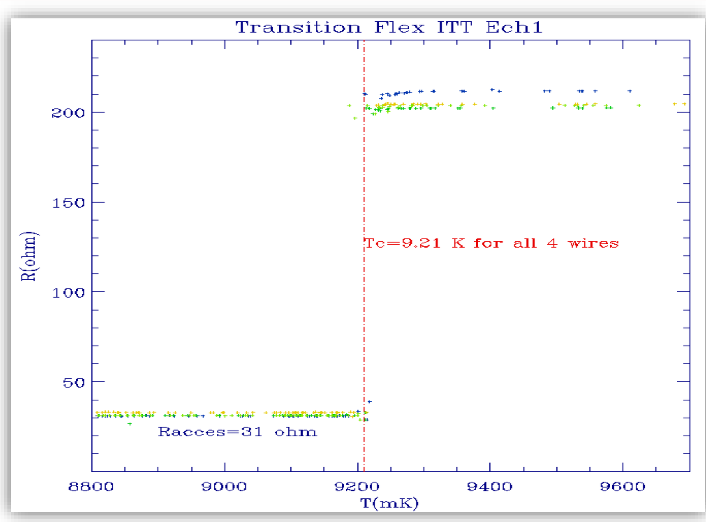
Zoom on a top thermal contact. Vias connect it to the two shielding plans. *Wire bonding pads ; the polyimide opening is visible (Variant 4).*

- **Next steps :**
  - Implementation of interconnections : multi-wire bonding (to minimize contact resistance), or soldering of SMD Nano-D connectors.
  - End of the systematical performance measurements.
  - Final version production.

Measurements

Electrical measurements

- **Critical temperature :**
  - Four-wires measurement of the electrical resistance of tracks, from one side of the flexible PCB to the other, when the temperature is varying (in both directions).
  - For the first realization (i.e. the monolayer flexible PCB), the critical temperature measured is ~8.5 K.
  - For the second realization (i.e. the multilayer flexible PCB), the critical temperature is 9.0 to 9,2 K, i.e. very close to that of the massive niobium (9.3 K). This excellent result is due to an improvement of the quality of the metals deposition.
- **Critical current :**
  - ≥ 100 mA (limit of the instrument) for the Variant 3 of flexible PCB.



Transition temperature measured on 4 wires. The residual resistance at low temperature is due to the access resistance of the measurement setup.

Thermal conductivity (arbitrary unit) of Variant 2 of the flexible PCB, versus the hottest side temperature (green), compared to that of a Manganin wire (l = 12 cm, ø = 0.13 mm) (red).

Thermal measurements

- **Thermal conductivity :**
  - The Variant 2 of the multilayer flexible PCB as been measured between a low temperature of 50 mK and a high temperature varying from 800 mK to 5 K (see plot at left).
  - For the moment, the measure is not absolute, but it can be compared to the conductivity of a Manganin wire (length 12 cm, diameter 0.13 mm) : both conductivities are comparable.
    An absolute measurement will be performed very soon.
- **Residual-resistivity ratio (RRR) :**
  It has been measured to ~3-4, which indicates a quite good metals deposition (it has doubled from first to second realization).