Fabrication and Characterization of (100) Silicon Membranes for a Multi-beam Superconducting Heterodyne Receiver

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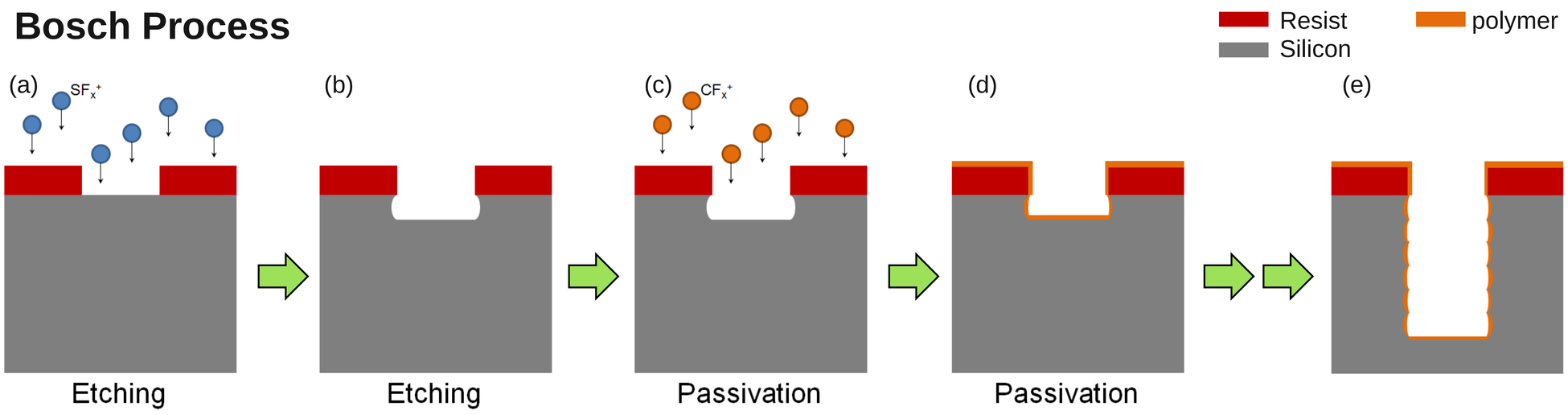
Introduction

Narrow field of view (FOV) is one of the significant limitations of a radio telescope for large area surveys. Aiming to extend the FOV of the radio telescopes, we started to develop the multi-beam superconducting heterodyne receiver which is highly compact and can accommodate more pixels than before. The concept for the multi-beam superconducting heterodyne receiver is implementing planar orthomode transducers (OMTs) and superconductor-insulator-superconductor circuits into an integrated circuit (IC). The fabrication of membranes is one of the most important techniques for these ICs, because the planar OMTs and wave probes that couples local oscillator power in the IC are fabricated on the membranes. As a pre-study before the IC fabrication, we fabricated (100) silicon membranes of 3 mm in diameter on the surface of silicon on insulator substrates, and the characteristics of the membranes were investigated.

Deep Reactive Ion Etching

Bosch Process

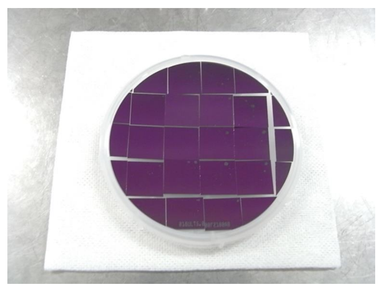


Bosch process is one of the deep silicon etching process for nearly vertical structures. It alternates repeatedly between isotropic plasma etch with SF_6 [(a), (b)] and deposition of an inert passivation layer with C_4F_8 [(c), (d)].

Specimens

Silicon on Insulator Wafer

Device layer (Silicon, 6 μm)
BOX layer (SiO_2, 1 μm)
Handle layer (Silicon, 400 μm)



Photograph of 3 inch silicon on insulator (SOI) wafer which cut in 15 mm square.

Experiments

Membrane Fabrication

Deep RIE equipment
MUC-21 Ase-Pegasus-Starlight (SPP Technologies Co.)

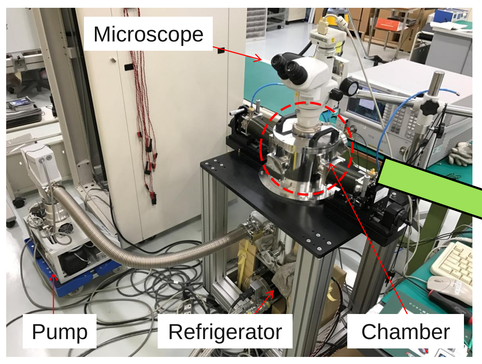
Deep RIE Process : Etching process for handle layer (silicon)

<Etch> SF_6:500 sccm, 8.0 Pa, Coil:2200 W, Bias:140 W, 2.0 sec.
SF_6:500 sccm, 22.0 Pa, Coil:2200 W, Bias:20 W, 7.0 sec.
<Pass.> C_4F_8:400 sccm, 10.0 Pa, Coil:2200 W, Bias:0 W, 2.0 sec.

SiO_2 Etching Process : Etching process for BOX layer

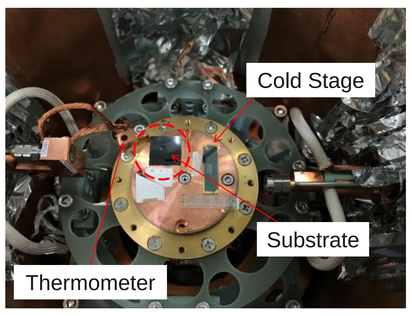
C_4F_8:25 sccm , Ar: 25 sccm, 1.0 Pa, Coil: 1400 W, Bias: 150 W

Cooling Test



Cooling System

Room Temperature > T > 4 K

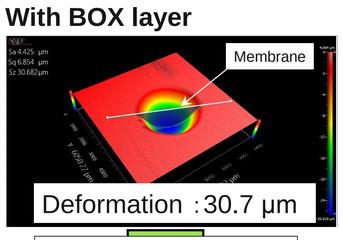


Inside of Chamber

Experimental Results

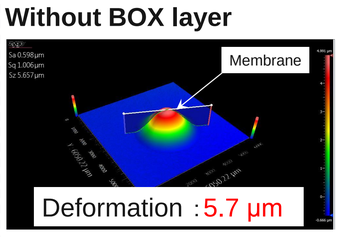
Membrane Surface

With BOX layer



BOX Layer Etching

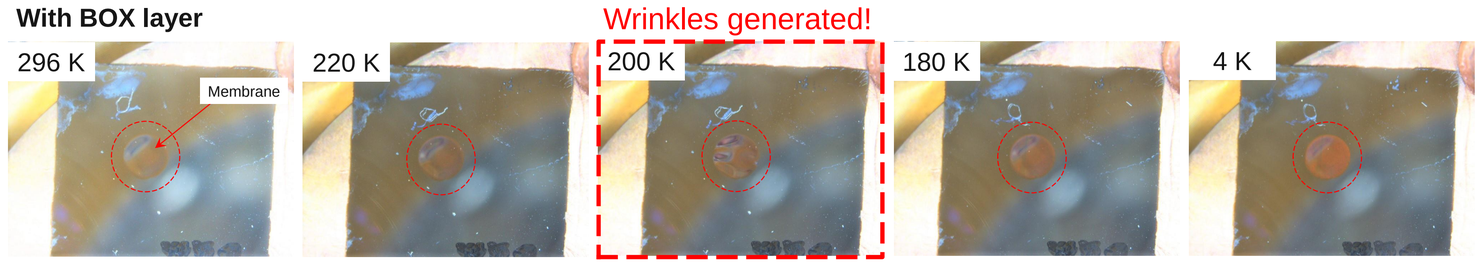
Without BOX layer



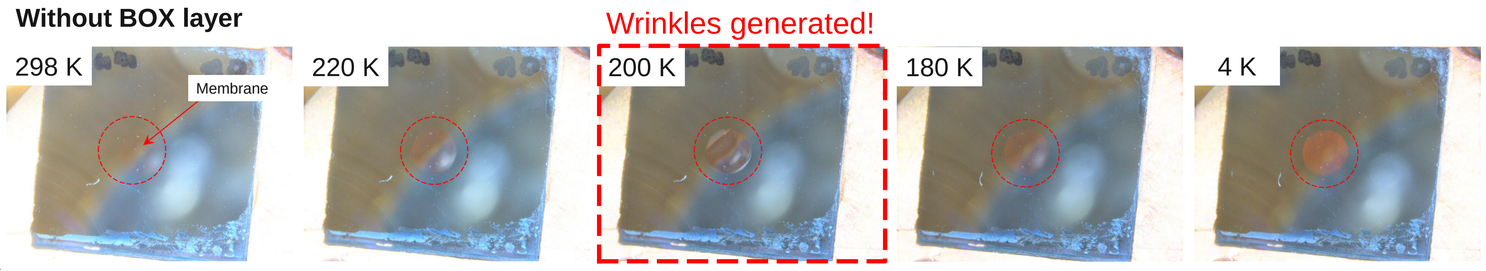
Membrane was Flattened!

Results of Cooling Tests

With BOX layer



Without BOX layer



Wrinkles structure was generated on both (100) silicon membranes near 200 K and disappeared below 180 K. This phenomenon would be related with device layer rather than BOX layer, because it was occurred in both (100) silicon membrane with and without BOX layer. According to some researchers, (100) silicon has the phase transition from c(4x2) to (2x1) near 200 K*.

* T. Tabata, et. al., Surf. Sci. **179**, L63 (1987).

Summary

We fabricated the membranes 3 mm in diameter on the SOI substrates using Deep RIE equipment. The handle layer of one SOI substrate was etched using Bosch process with the BOX layer remained. The BOX layer of the other SOI substrate was removed using C_4F_8 based plasma etching after the handle layer etching. The (100) silicon membranes with the BOX layer and without the BOX layer have the ark-like deformation with maximum height of 30.7 μm and 5.7 μm, respectively. It shows the (100) silicon membranes of SOI substrates are effectively flattened by etching the BOX layers under the (100) silicon device layers. Both (100) silicon membranes were cooled from room temperature to 4 K by the GM refrigerator. Wrinkles structure was generated on both (100) silicon membrane near 200 K. However the wrinkles structure of the (100) silicon membrane was disappeared below about 180 K.